





FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO. MP0088	APPLICATION NO. 09/920,241
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT Pierte ROO	
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DATE SUBMITTED TO USPTO: August 11, 2005			
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21	Razavi, Principles of Data Conversion System Design		
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21	Gotoh, et al., All-Digital Multi-Phase Delay Locked Loop for Internal Timing Generation in Embedded and/or High-Speed DRAMS		
21	Johnson, et al., THAM 11.2: A Variable Delay Line Phase Locked Loop for CPU-Coprocessor Synchronization		
21	Sonntag, et al., FAM: 11.5: A Monolithic CMOS 10MHz DPLL for Burse-Mode		
01	Garlepp, et al., A Portable Digital DLL Architecture for CMOS Interface Circuits		
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21	Dehng, et al., A Fast-Lock Mixed-Mode DLL Using a 2-b SAR Algorithm		
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Pierre ROO

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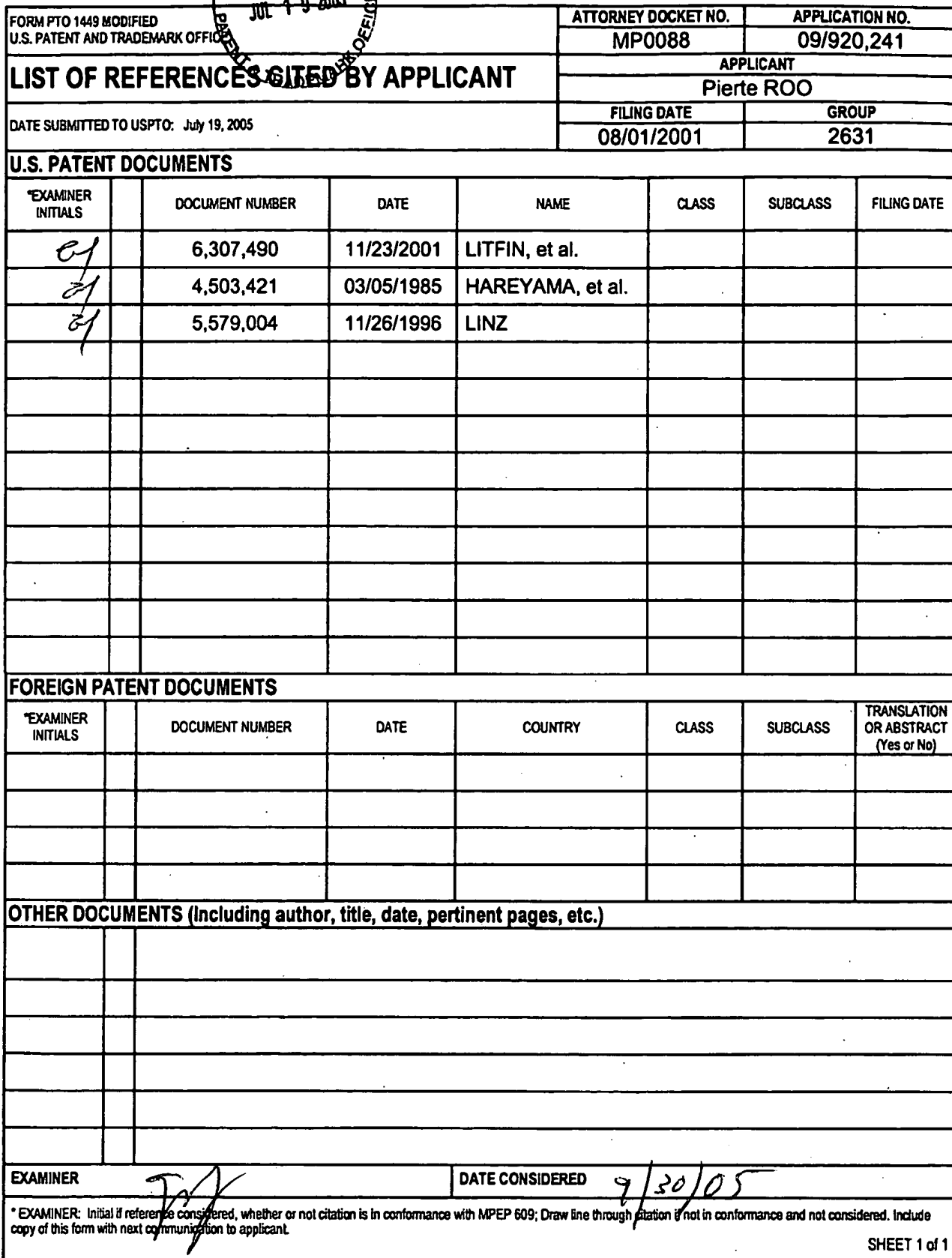
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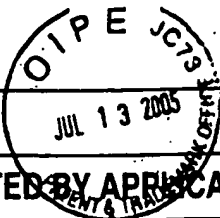
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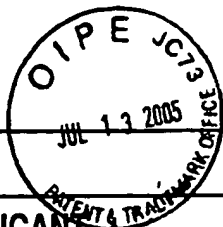
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APPLICATION NO.

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APPLICANT

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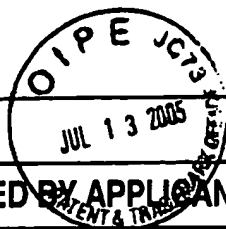
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ATTORNEY DOCKET NO.

APPLICATION NO.

MP0088

09/920,241

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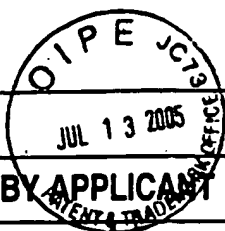
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81	4,972,360	11/20/1990	Cukier et al.			
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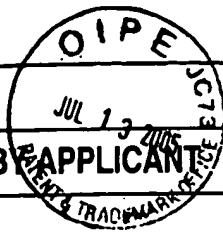
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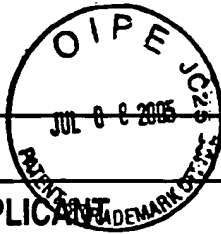
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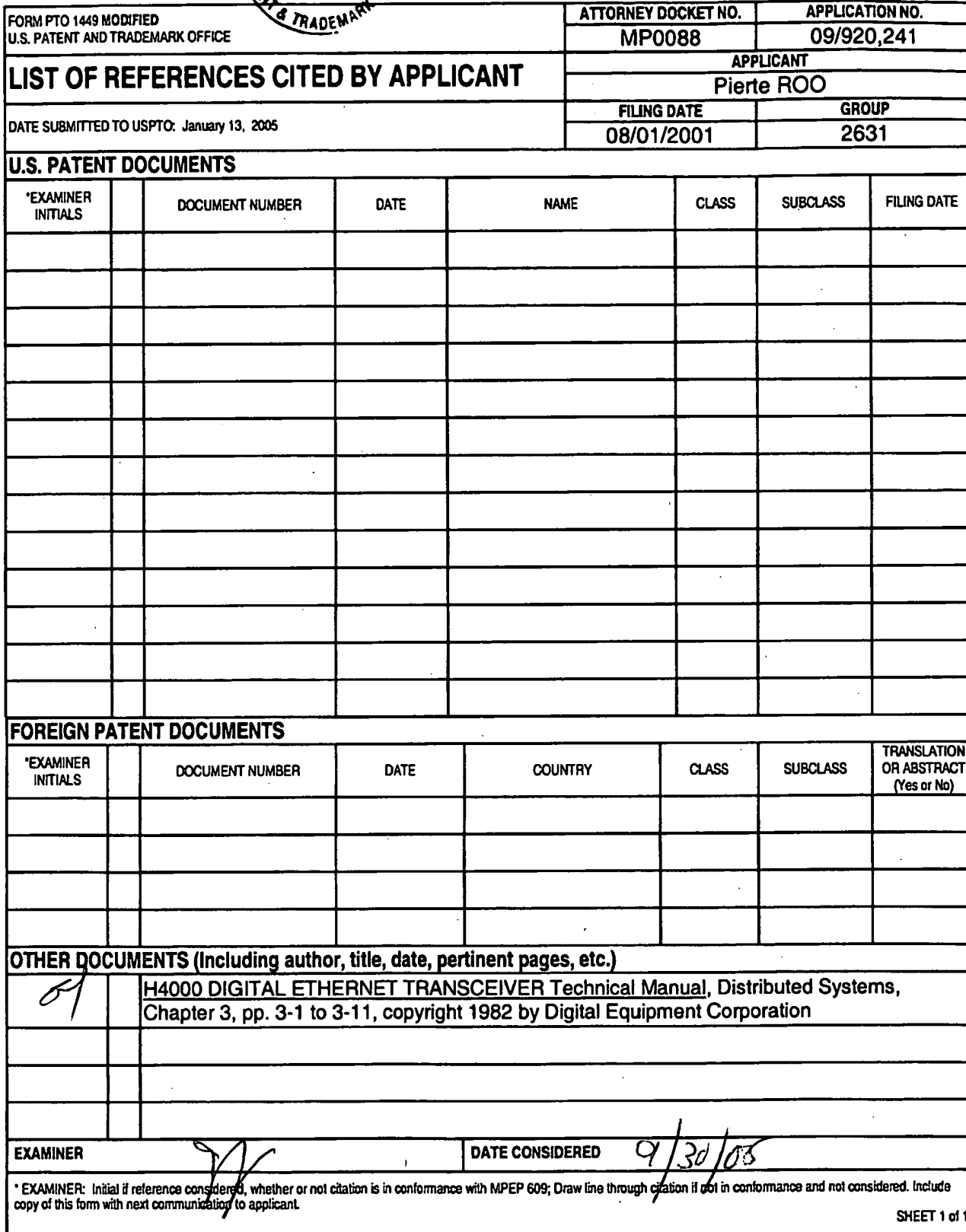
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FILING DATE

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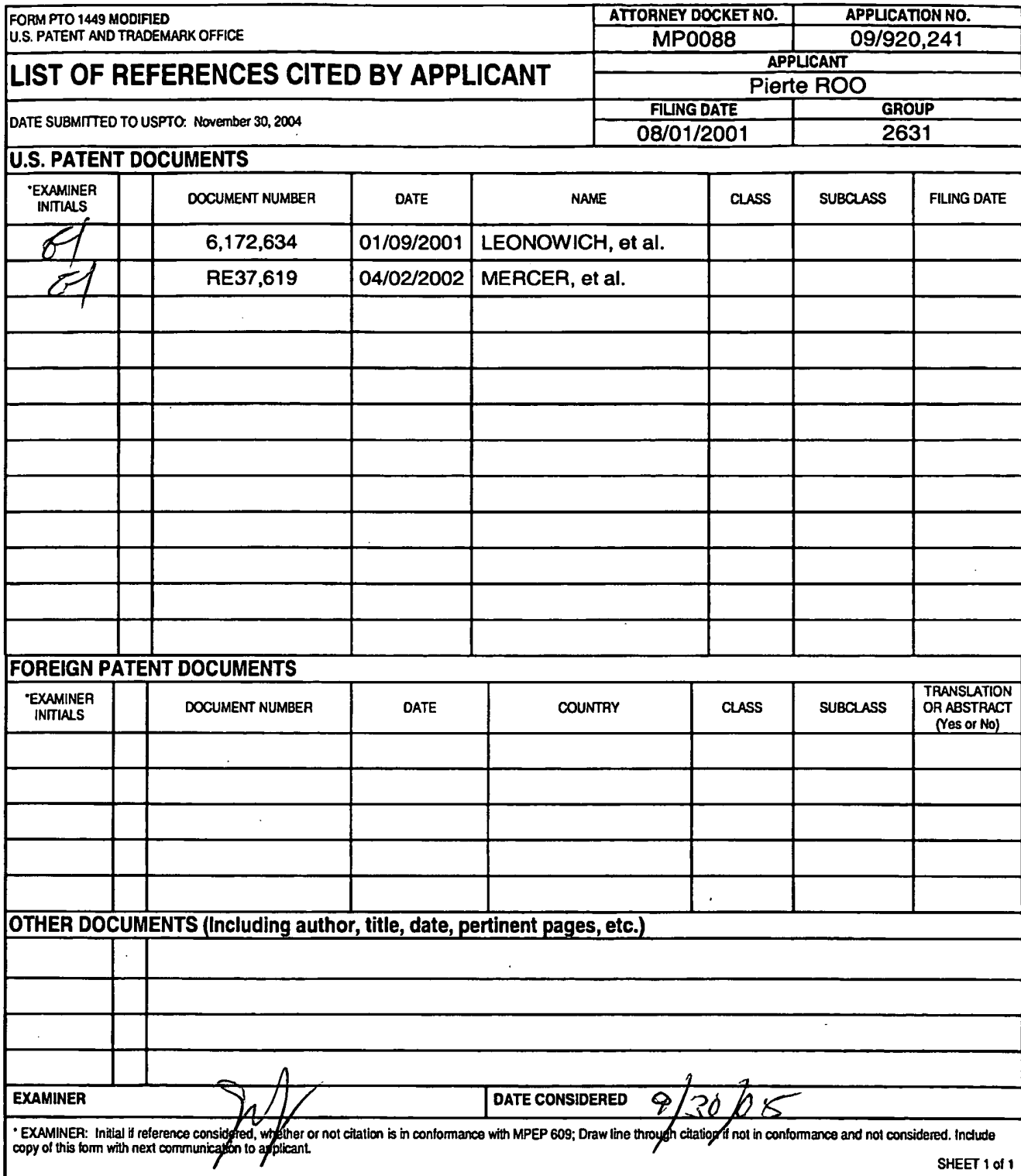
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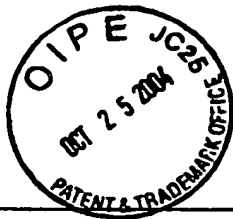
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*EXAMINER INITIALS		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT (Yes or No)
OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)							
21		THE ELECTRICAL ENGINEERING HANDBOOK, Chapter 31, "D/A and A/D Converters", Richard C. Dorf, editor, CRC Press, 1993					
EXAMINER		DATE CONSIDERED		9/30/05			
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							
SHEET 1 of 1							

Form PTO-1449

**INFORMATION DISCLOSURE CITATION
IN AN APPLICATION**

(Use several sheets if necessary)

Docket Number
13200-00074Application Number
09/920,241Applicant
Pierte RooFiling Date
August 1, 2001Group Art Unit
Not yet known**U. S. PATENT DOCUMENTS**

EXAMINER INITIAL	DOCUMENT NUMBER							DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROP.
81	R	E	3	0	1	1	1	10/09/79	Blood, Jr.	178	58 R	
	4	1	1	2	2	5	3	09/05/78	Wilhelm	178	58 R	
	4	1	5	2	5	4	1	05/01/79	Yuen	178	59	
	4	3	9	3	4	9	4	07/12/83	Belforte et al.	370	27	
	5	3	0	7	4	0	5	04/26/94	Sih	379	410	
	5	3	8	8	0	9	2	02/07/95	Koyama et al.	370	32.1	
	5	5	1	7	4	3	5	05/14/96	Sugiyama	364	724.19	
	5	5	3	9	7	7	3	07/23/96	Knee et al.	375	232	
	5	6	5	9	6	0	9	08/19/97	Koizumi et al.	379	410	
	5	6	6	6	3	5	4	09/09/97	Cecchi et al.	370	284	
	5	7	9	6	7	2	5	08/18/98	Muraoka	370	290	
	5	8	2	2	4	2	6	10/13/98	Rasmus et al.	379	402	
	5	8	2	5	8	1	9	10/20/98	Cogburn	375	257	
81	5	8	6	4	5	8	7	01/26/99	Hunt	375	316	

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	Translation	
						Yes	No
81	WO 99/46867	09/16/99	PCT				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

81	"Microelectronic Circuits," Third Edition, Sedra et al., Chapter 2: Operational Amplifiers, §2.4, pp. 61-63, 1991.

EXAMINER

DATE CONSIDERED

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